無線通訊系統之積體電路設計(II)

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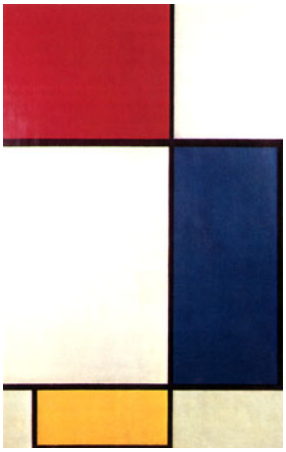


Outline

- Introduction of Wireless Communication System
- Analog Filter Design
- Switched Capacitor Filter Design
- Digital to Analog Circuit Design
- S/H Circuit Design
- Analog to Digital Circuit Design
- Appendix

Digital to Analog Circuit Design

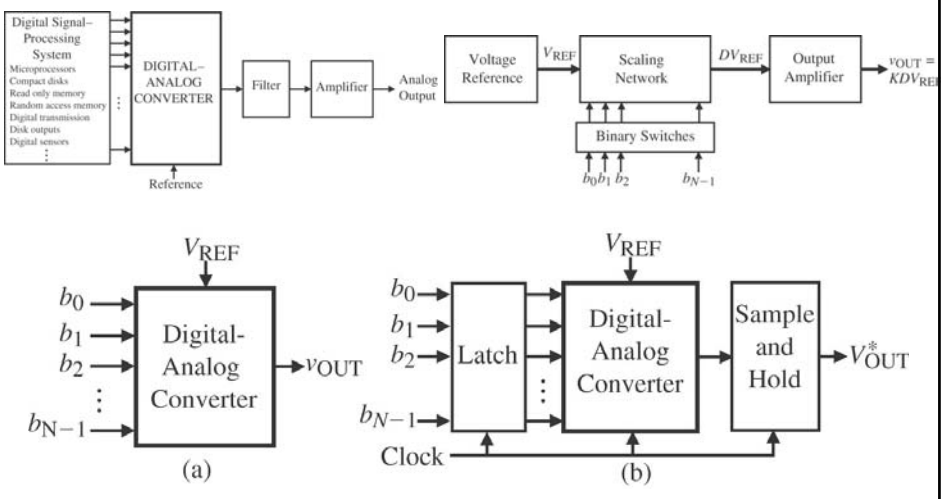
Data Converter

- *Data Converter of ADC and DAC: Provide interfaces between the analog environment (the physical world) and a digital environment.*
- *Can be monolithically integrated with digital VLSI circuits for digital signal and data processing functions.*
- *Digital VLSI (DSP) Circuits are better in* :
  - *Accuracy.*
  - *Design Flexibility.*
  - *Reliability.*
  - *Programmability.*
  - *Reproducibility.*
  - *Cost and Chip size Down* (*Portable*).
  - *Immunity to Process Variation, and Temperature and Voltage Drift.*
- *Data Converter Consideration :*
  - *Bandwidth (Speed) limitation.*
  - *The Finite Word length* (*8, 16, 32-bits*) effect.

Nyquist-Rate Data Converters :

- Nyquist-Rate Converters:.
  - ✓Generate uniquely a series of output for each input with *one-to-one* correspondence.
  - ✓Seldom used at the Nyquist rate due to the difficulty in realization of anti-aliasing and reconstruction filters.
  - ✓Operate at 1.5~5 times the Nyquist rate. That is 3 to 10 times the input signal's bandwidth.

DAC Structure



Ideal DAC and Transfer Curve

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Nyquist-rate DAC: convert a digital (binary) input signal (or code) to an analog output voltage (or current) that is proportional to the digital signal.

DSP system output

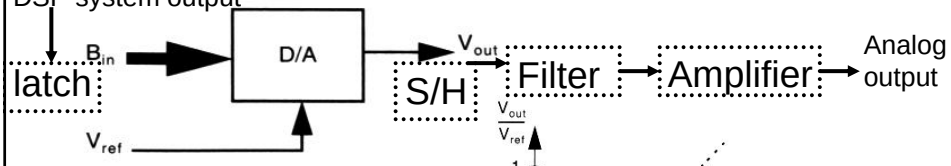

Fig. 11.1 A block diagram representing a D/A converter.

If No noise and any imperfection condition:

MSB LSB

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) = V_{ref} B_{in}$$

$$V_{LSB} = \frac{V_{ref}}{2^N},\ 1\,\text{LSB} = \frac{1}{2^N}$$

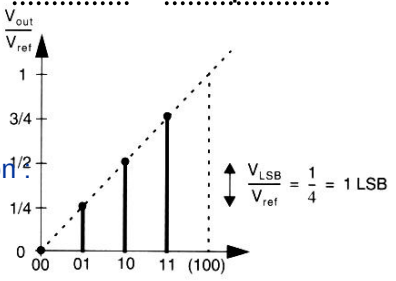

Fig. 11.2 Input-output transfer curve for an ideal 2-bit D/A converter.

Max output: Vref $(1-2^{-N})$

Ideal ADC and Transfer Curve

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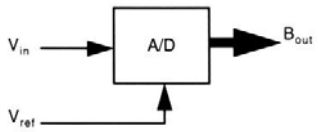

Fig. 11.3 A block diagram representing an A/D converter.

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) = V_{in} \pm V_X$$

where, $-\frac{1}{2}V_{LSB} \le V_X < \frac{1}{2}V_{LSB}$

$-(1/2^N)Vref < Vin < Vref\ (2^{N-1}/2^N)$

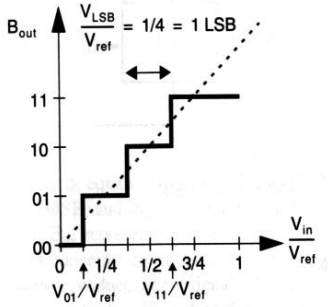

Fig. 11.4 Input-output transfer curve for a 2-bit A/D converter.

- Overloaded in Converter: The magnitude of the quantization error is larger than $V_{LSB}/2$.
- Quantization Error: a range of valid input values that produce the same digital output word.

Quantization Noise and Deterministic Approach

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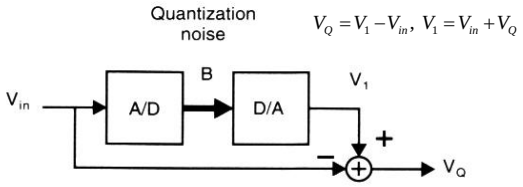

Fig. 11.5 A circuit to investigate quantization noise behavior.

V_1: Quantized Signal.
V_Q: Quantization Noise Signal, is limited to $\pm V_{LSB}/2$. The average of V_Q is zero.

For deterministic ramp input:

$$V_{Q(rms)} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2 dt\right]^{1/2} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2 (\frac{-t}{T})^2 dt\right]^{1/2}$$

$$V_Q = \left[\frac{V_{LSB}^2}{T^3}(\frac{t^3}{3}\Big|_{-T/2}^{T/2}\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

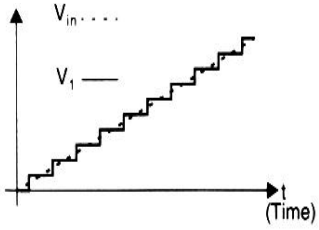

Fig. 11.6 Applying a ramp signal to the circuit in Fig. 11.5.

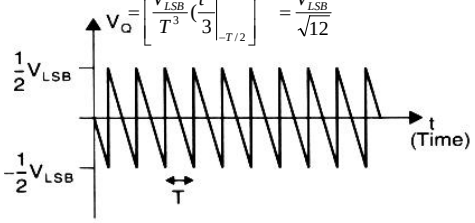

Fig. 11.6 Applying a ramp signal to the circuit in Fig. 11.5.

Quantization Noiseand ENOB

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For *saw tooth* Vin of Vref:

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(2^N\right) = 6.02\text{N } dB$$

For *sinusoidal* Vin of Vref:

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\sqrt{\frac{3}{2}}2^N\right) = 6.02\text{N} + 1.76 \quad dB$$

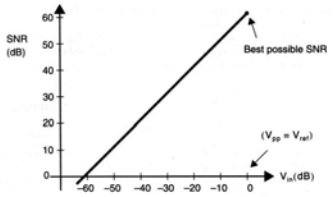


Fig. 11.8 Idealized SNR versus sinusoidal input signal amplitude for a 10-bit A/D converter. The 0-dB input signal amplitude corresponds to a peak-to-peak voltage equaling V_{ref}.

$$ENOB = \frac{SNR_{actual} 1.76}{6.02}$$

Performance Limitations : Gain and Nonlinear Error

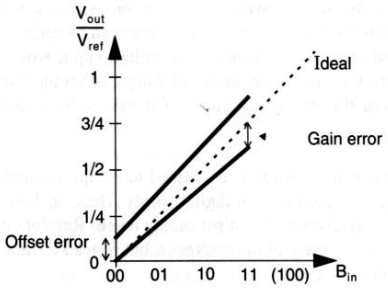


Fig. 11.9 Illustrating offset and gain errors for a 2-bit D/A converter.

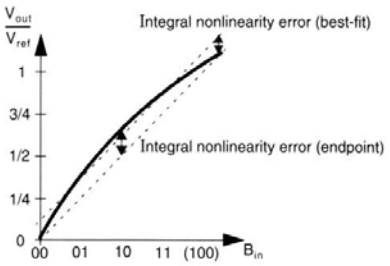


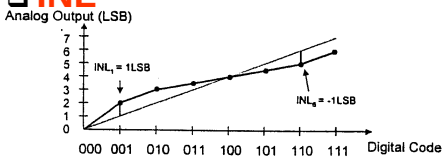
Fig. 11.10 Integral nonlinearity error in a 2-bit D/A converter.

Gain error:

the change in the slope of the transfer characteristic (due to the inaccuracy of the scale factor or reference voltage).

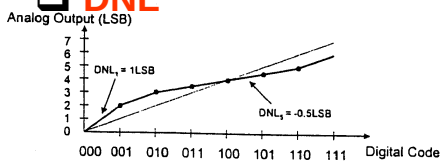
Performance Limitations : DNL/INL

❑ INL



- $INL_i = V_{real}(i)/LSB - i$, $i = 0 \ldots 2^n-1$; $(V_{real}(i)-V_{ideal}(i))/LSB$
- $INL = Sign(INL_i)Max.(|INL_i|)$, $i = 0 \ldots 2^n-1$

❑ DNL



- $DNL_i = (V_{real}(i) - V_{real}(i-1))/LSB - 1$, $i = 0 \ldots 2^n-1$
- $DNL = Sign(DNL_i)Max.(|DNL_i|)$, $i = 0 \ldots 2^n-1$

- ❑ The linearity is a measure of the nonlinearity error at the output after the offset and gain errors have been removed.
- ❑ *Integral Nonlinearity (INL)* : the *maximum difference between the actual finite resolution characteristic* and the ideal finite resolution characteristic measured vertically (the endpoints of the transfer characteristic vertically).
- ❑ *Differential Nonlinearity (DNL):* is the measure of the *separation* between adjacent levels measured at each vertical jump and specified as a fraction of LSB.

DNL/INL Testing

- **INL :**

Ramp the DAC input from 00000000~111111111, so we can get the DAC output from *black level to white level*.

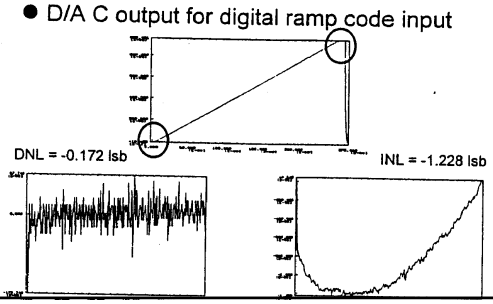
LSB = (White – Black)/511

INL = MAX{DAC(i) – LSB x i } , i=0~511

- **DNL :**

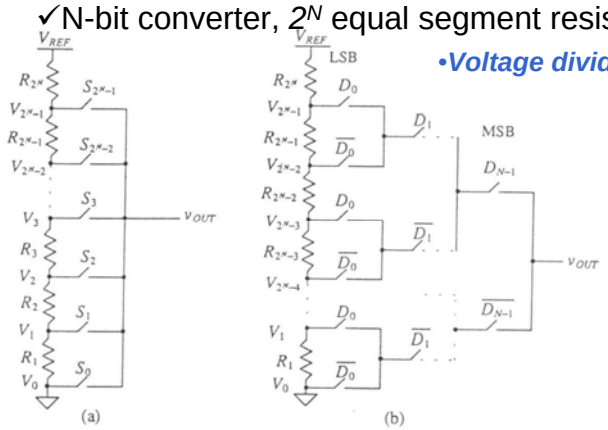
Use the same DAC(i) output step voltage measurements for INL to calculate the DNL : DNL = MAX{DAC(i) – DAC(i-1) - LSB} , i=0~511

$$DNL = (\frac{V_{cx} - V_s}{V_s}) \times 100\% = (\frac{V_{cx}}{V_s} - 1) LSBs$$



Resistor String (Voltage-Scaling) DAC

- **Simplest** voltage-reference divider.
- *Tree-type* ***Resistor-String*** (*Voltage-Scaling*) *DAC* :
  - ✓N-bit converter, 2^N equal segment resistors for each LSB.
  - ***•Voltage divider (Decoder-based) DAC.***



$$V_{i,OUT} = V_{REF} \cdot \frac{\sum_{k=1}^{i} R_k}{\sum_{k=1}^{2^n} R_k}$$

Resistor-String DAC

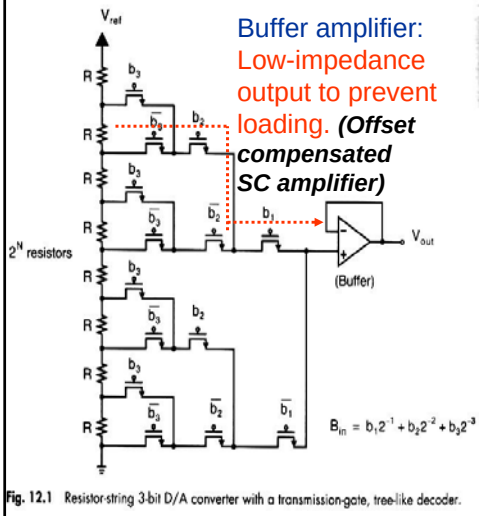


Fig. 12.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder.

Buffer amplifier: Low-impedance output to prevent loading. ***(Offset compensated SC amplifier)***

- ***Segmented resistor string of switch network.***
- ***Switch: CMOS transmission gate.***
- **Regular structure** (well-suited for MOS technology).
  ⇒ ***Compact Layout.***
- ***Monotonicity :***
  - ✓ ***Accuracy dependent on the matching accuracy of R.***
  - ✓ ***Poly-resistor ≈20~30 Ω/□ .***
  - ⇒ **At most 10 bit accuracy.** (***because the bit number ↑, the RC-delay ↑ and limit the DAC speed).***

Resistor-String DAC Design

- Guarantee *monotonicity* since voltage at each tap cannot be less than the tap below.
- Equal segment resistors (Diffusion Poly-Si strip). ⇒ Good *differential linearity*.
- To insure max uniformity of step size, *Linearity*, the R_{on} of the Switch (transmission gate) should be made as large as possible! ⇒ ***but must trade off the Resistive loading.***
- Speed : ***The delay through the switch network is the major limitation on speed.*** ⇒ **Also** from the C_{para} at each node of resistors.
  - ✓ the R_{on} of Switch (binary code-dependent settling time).
  - ✓ Only Larger *Capacitive Loading at* the output node (No resistive Loading).
  - ✓ the operating speed (bandwidth) of the *output buffer*.

Resistor-String DAC

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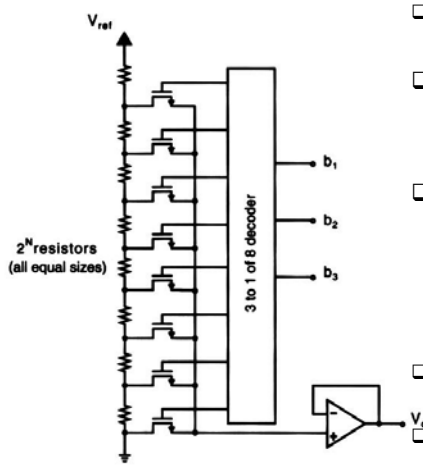

Fig. 12.3 Resistor-string 3-bit D/A converter with digital decoding.

- *Large Capacity and More Area for the digital decoder circuits.*
- *Advantages :*
  - ✓ *Inherently Monotonic.*
  - ✓ *Small area for resolution < 8 bits.*
- *Disadvantages :*
  - ✓ Large area for *resolution < 8 bits.*
  - ✓ *Susceptible to Process Gradients.*
  - ✓ *Susceptible to Contact Resistance.*
  - ✓ *Susceptible to Voltage Coefficient.*
- *DNL depends on local matching of neighboring R's.*
- *INL depends on global matching of R's.*

Current Scaling (Current Steering) DAC

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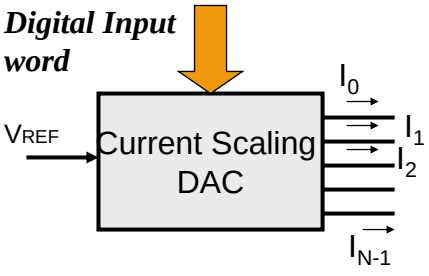
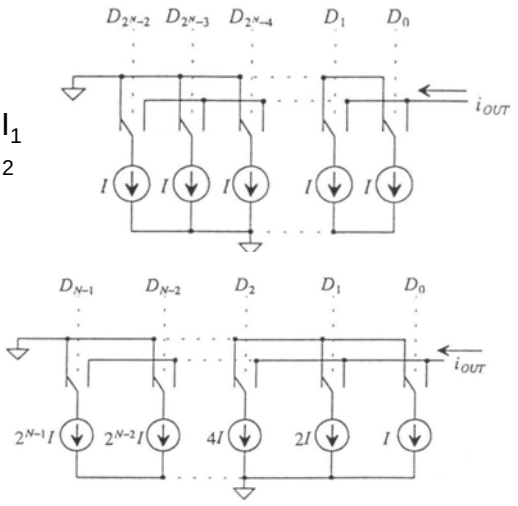


-*Weighted Current Sources*



Binary-Weighted Current Scaling DAC Converters

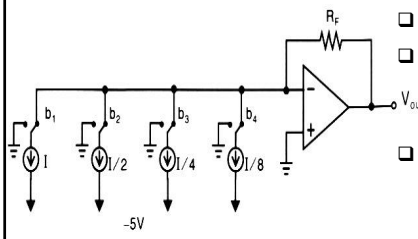


Fig. 12.13 Binary-weighted current-mode D/A converter.

- **Higher speed operation.**
- **Binary weighted.**
- For 10~20 um feature size, 0.2%~0.5 % matching accuracy. ⇒ ***10-bit level at most***.
- Difficult to design in the higher resolution :
  - ✓ **Must synchronize the input Digital code.**
  - ✓ **Ro of the current source will make nonlinearity (DNL and INL).**
  - ✓ **Too many current sources and large area.**
  - ✓ **Large resistor, wide range transistor size.**

  ⇒ **these above consideration will limit the *temperature stability* and *speed*.**

The Binary-Weighted Current-Switched DAC Design

- *Current-Switched DAC* :***Simple*** and ***high speed***.
- ***Advantages*** :
  - ✓ ***Inherent high speed.***
  - ✓ ***Easy to generate Nonlinear data transfer.***
  - ✓ ***Easy to segment.***
  - ✓ ***Easy to Self-Calibration.***
- ***Disadvantages*** :
  - ✓ **Large glitches due to timing skews.**
  - ✓ **INL depends on different transistor Matching.**
  - ✓ **Critically dependent on Rout of current source device.**

Binary-Scaled (Current Scaling) Converter

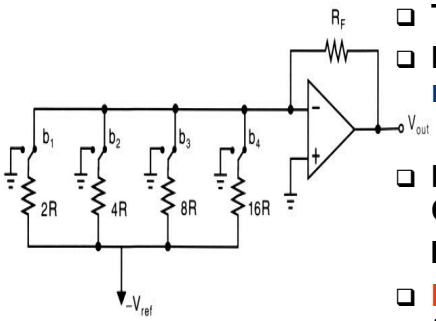


Fig. 12.7 Binary-weighted 4-bit resistor D/A converter.

- The *most popular* approach.
- Binary array signal is current (in resistor or current).
- Binary-weighted resistor Converter:

  $Bin= b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + b_4 2^{-4} + \ldots$
- Large component spread leads to poorer matching between resistors and maybe require trimming for MSB resistor.
- Prone to *glitches* for high speed applications.

Reduced-Resistance-Ratio Ladder

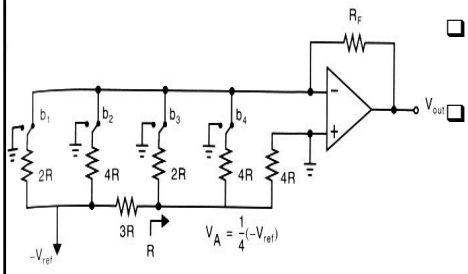


Fig. 12.8 Reduced-resistance-ratio 4-bit D/A converter.

- The current ratio has remained unchanged.
- Inserting the series resistor-3R for reducing the larger resistor ratio.

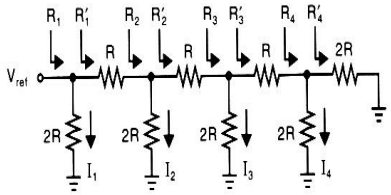


Fig. 12.9 R-2R resistance ladder.

- *R-2R method:* Smaller size and better matching accuracy than a binary-sized DAC.
- $R_4'=2R$, $R_4=R$, $R_3'=2R$, $R_3'=2R$

  $\Rightarrow$ $I_1=V_{ref}/2R$, $I_2=V_{ref}/4R$, $I_3=V_{ref}/8R$, $I_r=V_{ref}/2R$.

4-bit R-2R-based (Current Scaling) DAC

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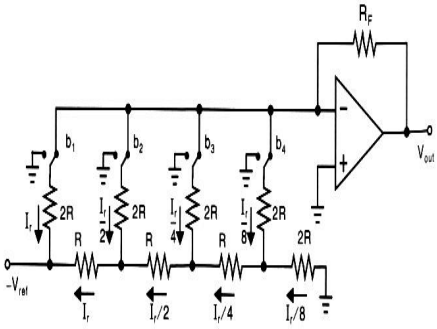

Fig. 12.10 4-bit R-2R based D/A converter.

- $I_r = V_{ref}/2R$.
- Widely varying current levels.

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref} \frac{R_F}{R} \sum_{i=1}^{N} \frac{b_i}{2^{i-1}}$$

4-bit R-2R-based DAC

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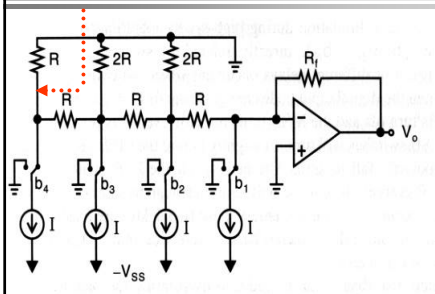

Fig. 12.11 R-2R ladder D/A converter with equal currents through the switches.

- The resistor seen to the left of any of the vertical 2R resistors is 2R.
- Only *three equal resistors*. ⇒Reduce the Current Ratio and good matching.
- Equal current to all switches.
- Slower speed.
- Fully Differential structure for Current Scaling DAC design.

Charge Scaling DAC

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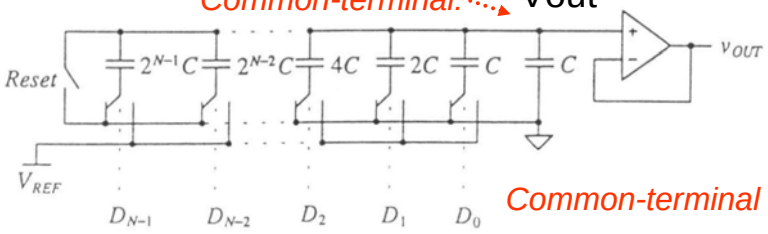
Q=CV

Common-terminal: Vout



Common-terminal poly-plate:

$$V_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \cdot V_{REF}$$

$C_2=C_1$
$C_3=2C_1$
$C_4=4C_1$
$C_5=8C_1$

45° for corner.

C5	C5	C4	C5
C4	C3	C2	C5
C5	C1	C3	C4
C5	C4	C5	C5

Common centroid arrangement:

The area-perimeter ratio is kept constant to prevent the *under cut*.

The Programmable Capacitor Arrays (PCAs)

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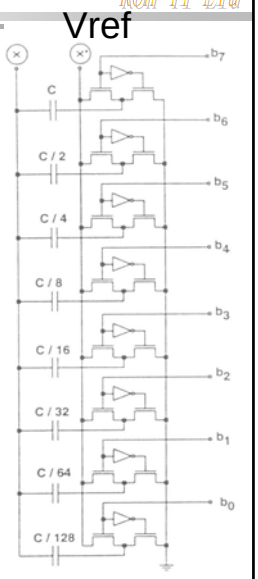
- The *Programmable SC Array circuits.*
- Very good *matching accuracy* for voltage and temperature coefficients.
- Binary (digitally variable) control signal: b0, b1, ... , b7.
- The *total capacitance* between x and x' :

$$C_t = \sum_{i=0}^{7} \frac{C}{2^{7-i}} b_i = 2^{-7} C \sum_{i=0}^{7} 2^i b_i$$



The Programmable Capacitor Arrays (PCAs)

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- Generally, largest number in a PCA is *6 ~10*.
- For n > 8, the *capacitance spread* C_{max}/C_{min} = 256, and the total capacitance C_t = 511 *C*.

  ⇒ 1. Capacitance spread inaccuracy (if *Cmin for LSB* is chosen too small)

  2. Excessive chip area. (if *Cmin* is chosen too large)
- The *common centroid layout* such as 12 um x 12 um *unit capacitor*.
- 10-bit level (1024 :1) matching accuracy:

⇒ For *Matching ratio 0.1 %*, the dimension is usually in the range of 20~30 um.

The Charge Scaling DAC

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- *Switched-induced errors* are cancelled by.
  - The *Offset* cancellation Op Amp by *Phase 1* and *Phase 2*.
  - In *Phase 1*, the control bits are applied.

Offset cancellation Op Amp

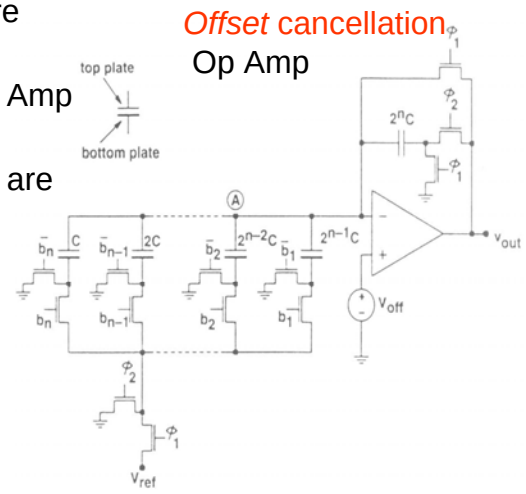


Figure 6.17. An *n*-bit charge-mode digital-to-analog converter.

$$V_{out} = -V_{ref} \sum_{i=1}^{n} b_i 2^{-i}$$

Bipolar Charge-Scaling DAC

Ron-Yi Liu

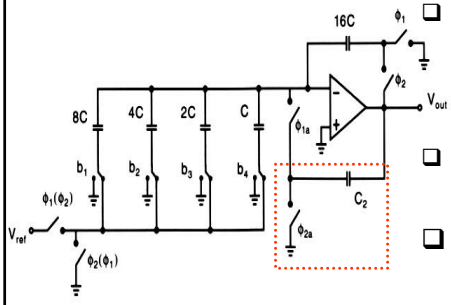


Fig. 12.12 Binary-array charge-redistribution D/A converter.

$$V_{out} = V_{ref}\sum_{i=1}^{n} b_i \frac{2^{-i}C}{16C} = V_{ref}\sum_{i=1}^{4} b_i \frac{2^{4-i}C}{16C}$$

- **SC offset-canceling amplifier : insensitive to Op Amp input-offset voltage, 1/f and finite Gain.**
- **Be careful in the clock generator design.**
- C2: as a deglitching capacitor for reducing the clock feed through.
- **ϕ_1: precharge phase:C, 2C, 4C, 8C to Vref. 16C reset.**
- **ϕ_2: evaluation Phase :**

Thermometer-code Charge Scaling DAC

Ron-Yi Liu

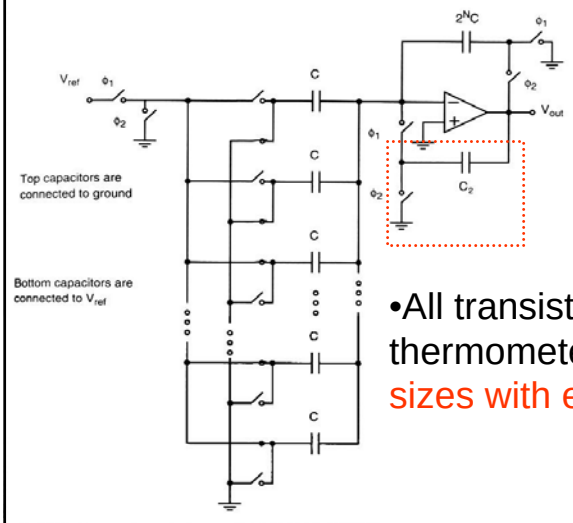


Fig. 12.16 Thermometer-code charge-redistribution D/A converter.

- All transistor switches in a thermometer-code are equal sizes with equal current.

The Segmented DAC Design

Ron-Yi Liu

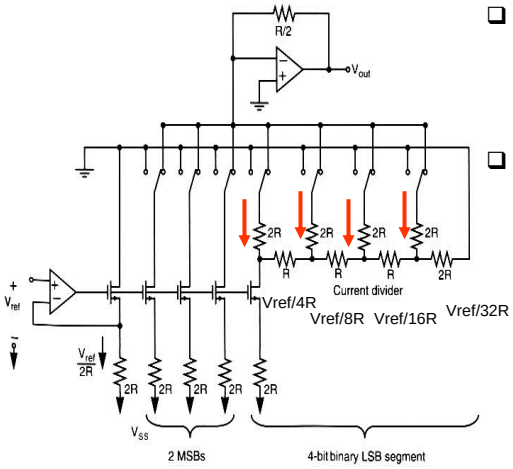


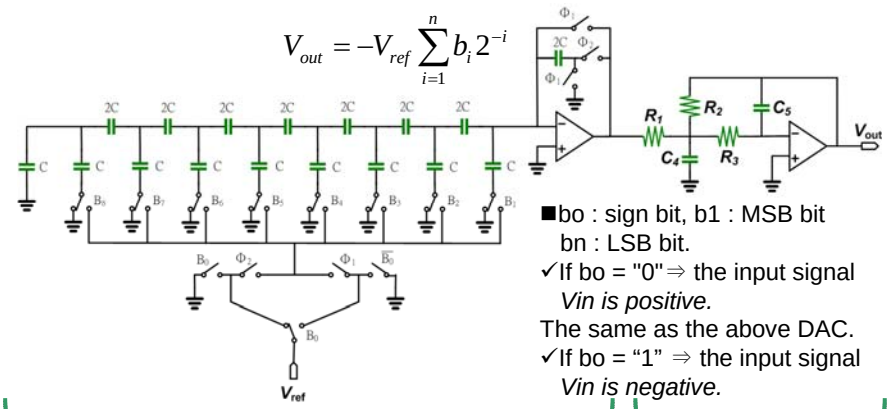
Fig. 12.22 A 6-bit segmented D/A converter.

- *The most popular design approach but not guaranteed to be monotonic*:
- 6 bits :
  - *4-LSB* segment is not *guaranteed to be monotonic (R-2R structure).*
  - *2-MSB* segment ; 3 equal current source using the thermometer-coding (less glitch).

0.18um 9b C2C DAC Chip Design

Ron-Yi Liu

$$V_{out} = -V_{ref} \sum_{i=1}^{n} b_i 2^{-i}$$



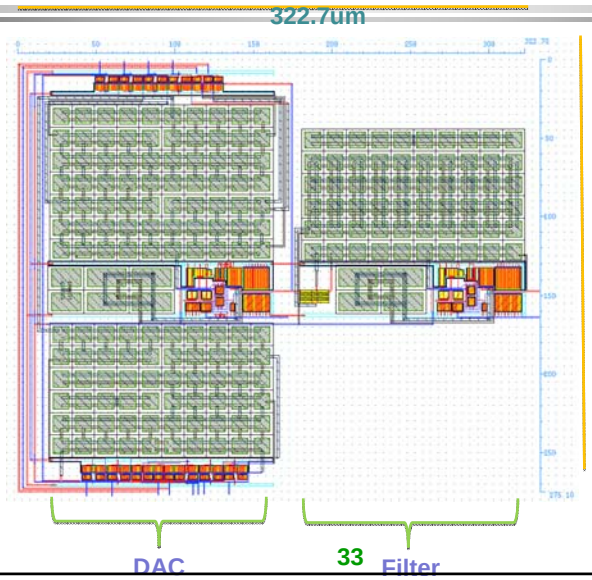
■bo : sign bit, b1 : MSB bit
bn : LSB bit.
✓If bo = "0"⇒ the input signal *Vin is positive.*
The same as the above DAC.
✓If bo = "1" ⇒ the input signal *Vin is negative.*

C-2C DAC **SALLEN-KEY FILTER**

C=0.5pf, CL=2pf, Fs=15MHz

C2C DAC Layout Diagram

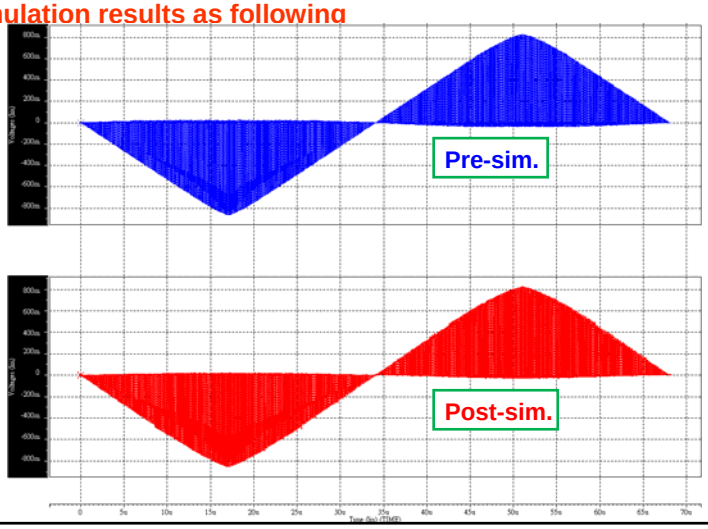
Ron-Yi Liu



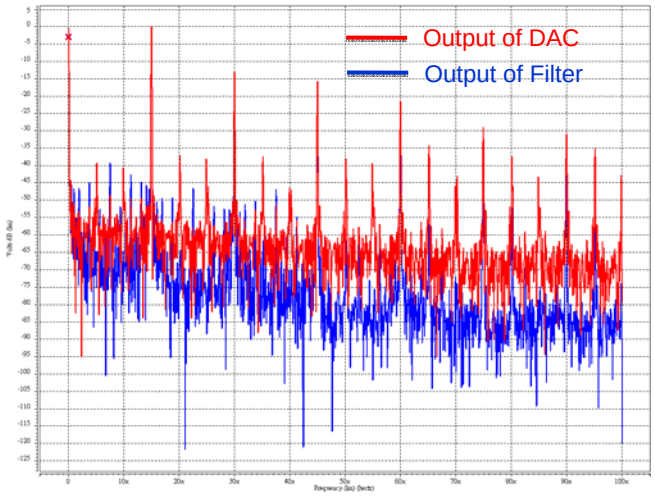
Output of C2C DAC Circuit

Ron-Yi Liu

- Giving an 8-bit digital signal to simulate an input of sine wave, and the simulation results as following



Post-Simulation Result of FFT



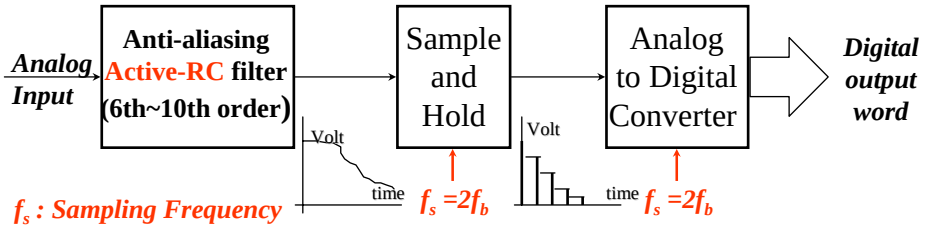
Sampler and Hold Circuit Design

The Conventional ADCs

1998/6/19

Ron-Yi Liu

❑*ADC : Essential building blocks in many* ***digital signal processing system*** *includes :* **one or more Comparators, switches, passive precision components, a precise voltage voltage reference and digital control logic.**



f_s : *Sampling Frequency*
f_b : *Signal Bandwidth*

The Resolution of classical data converter is 10~12 bit range :
⇐ ***limited by component matching and circuit nonlinearity.***

Sampler and Hold Circuits

2010/5/3

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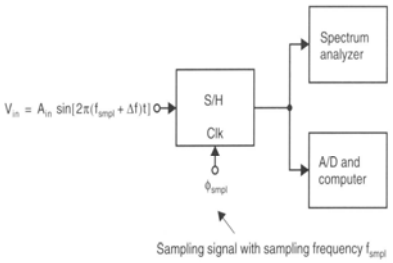


Fig. 8.1 The test setup for characterizing a sample and hold using a beat test.

❑***Sampler and Holder S/H (Track-and-Hold) circuits :***

- ***Sample analog signal and store for some time.***
- ***Applied in data-acquisition systems such as A/D converter.***

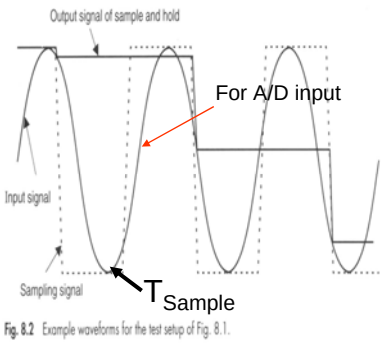


Fig. 8.2 Example waveforms for the test setup of Fig. 8.1.

- ***S/H Max clock frequency (Min conversion time) $f_{sample}=1/T_{sample}$.***
- ***Input signal slightly different clock frequency.***
- ***Small frequency difference to spectrum analyzer for beat testing.***

Switched Capacitor Sampler and Hold Circuits

Ron-Yi Liu

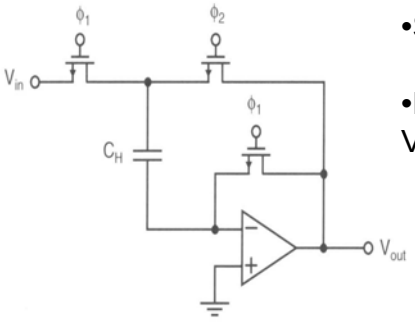


Fig. 8.15 A simple switched-capacitor S/H.

- •Sampling : C_H is charged by V_{in}-V_{os} and V_{out}=-V_{os}
- •Hold mode:
  V_{out}= (V_{in}-V_{os})-(-V_{os})=V_{in}

- **Quite accurate and Lower frequency: Vout≈0 in the sampling mode. ⇒ Sample and Hold circuits (not a Track-and–Hold circuits).**
- ***Higher slew rate Op Amp and Fully Differential structure..***

Switched Capacitor Sampler-Hold and Low Pass Filters

Ron-Yi Liu

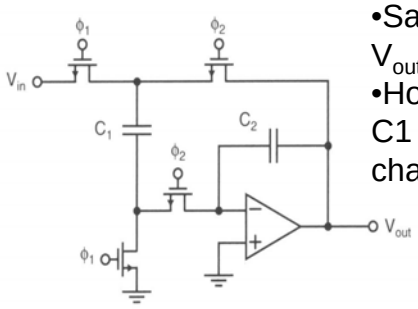


Fig. 8.19 A switched-capacitor sample and hold and low-pass filter.

- •Sampling : C_1 is charged by V_{in} and V_{out}=V_{in} (previous)
- •Hold mode: V_{out}= $V_{in}$and charge in C1 is shared with previously stored charges in C2.

- **For low frequency, Vout=Vin in the steady state. [scooch, 1991].**
- **Applied to convert High-quality Audio signal from SD domain to CT domain based Sigma-Delta DAC.**

- •If C2>> C1, the –3dB LP frequency is:

$$f_{-3dB} \cong \frac{1}{2\pi}\frac{C_1}{C_2} f_{CLK}$$

The input and output signal spectrum of Sampler and Hold Circuit

Ron-Yi Liu

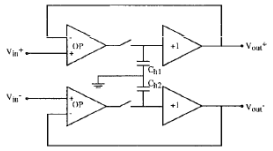


Figure 9: Pseudo-differential switched capacitor S/H

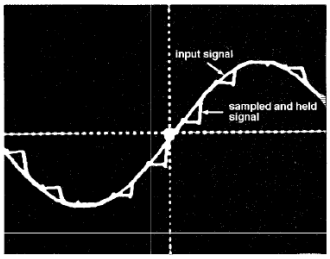


Figure 12: Measurement results for a sinusoidal input

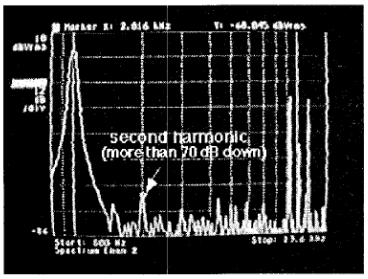
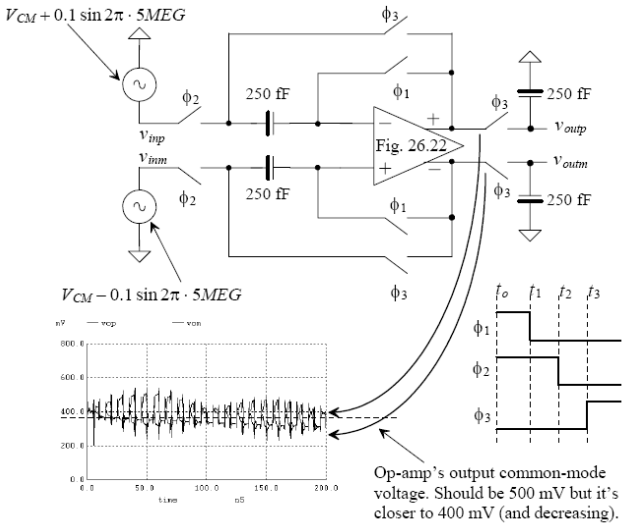


Figure 13: S/H sinusoidal signal spectrum

CMOS Sampler-Hold Circuit

Ron-Yi Liu



Sampler and Hold Circuit Simulation

2010/5/3

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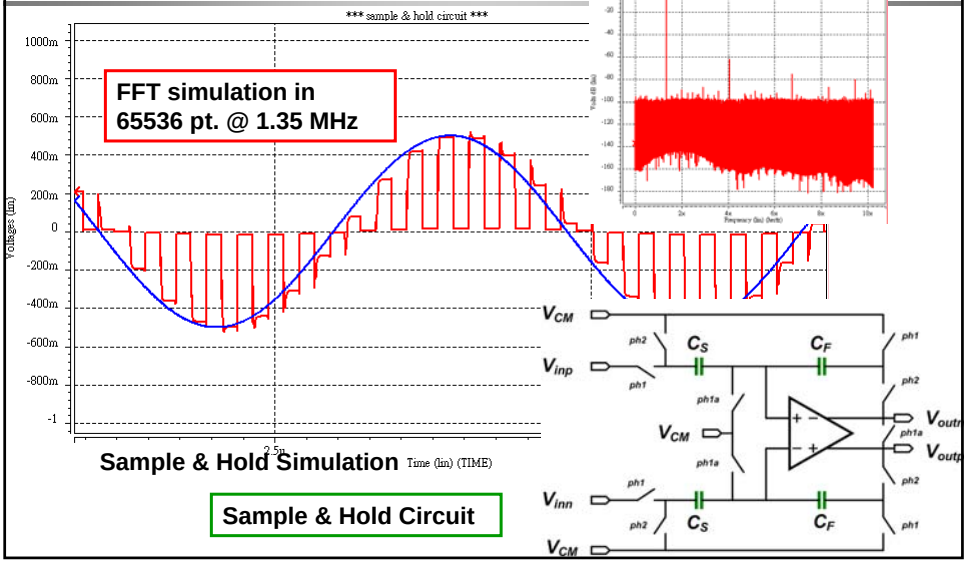
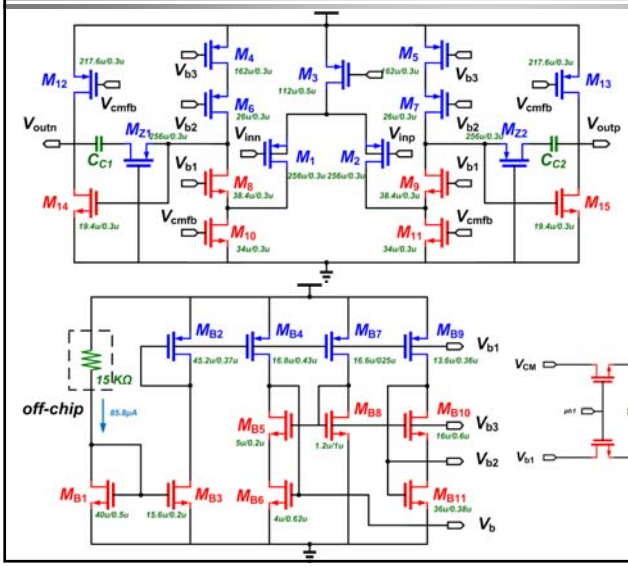


0.18um 1.8V Op Amp Design

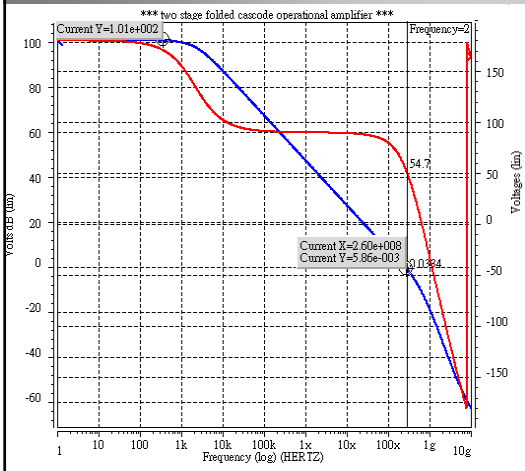
2010/5/3

Ron-Yi Liu

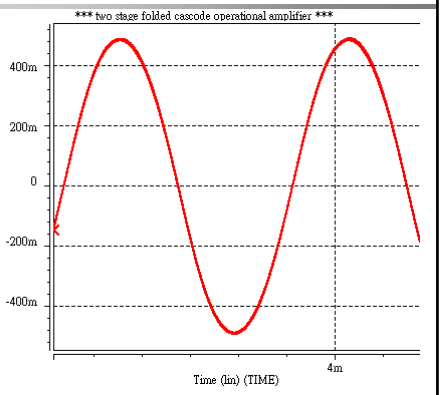


- A two stage Op Amp circuit with Miller compensation.
- Because of there are two stage in this design, two same CMFB circuits are applied.

CMOS Op Amp Simulation



DC Gain: 101 dB,
Phase Margin: 54.7˚,
Unity Gain Bandwidth: 260 MHz



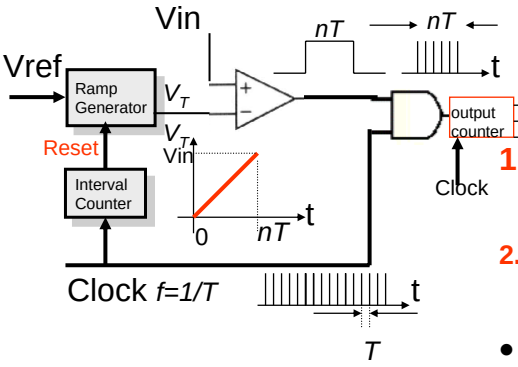
Transient Simulation

The output swing of this Op Amp circuit could able to swing to $1V_{p-p}$, but not distortion.

Analog to Digital Circuit Design

Single Ramp Integrating ADC Design

Ron-Yi Liu



- The inaccuracies from initial point, Vref, RC time constant,... ⇐ **Dual Ramp Integration ADC architecture.**

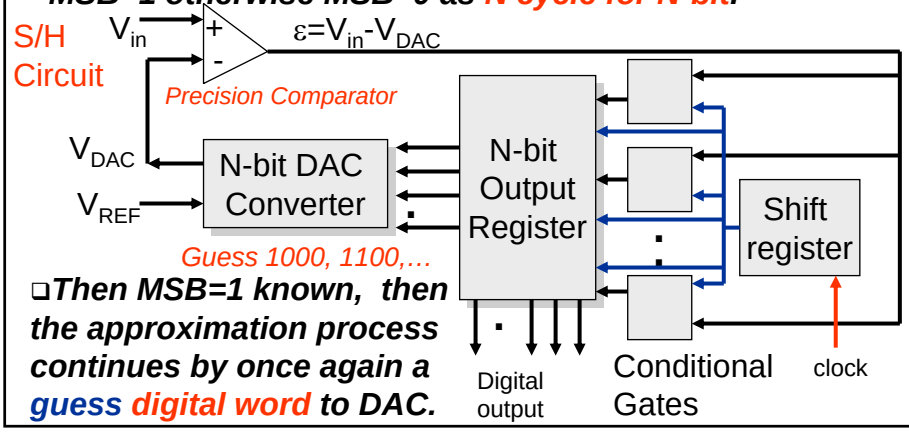
1. Transform input Vin to time interval (whose duration is proportional to signal).
2. convert the time duration into digital number by an accurate clock and digital counter.

- Adv : High accuracy and Simple operation.
- But low speed (long conversion time), and is easily subject to error in the ramp generator and Op Amp's Vos
- Only for unipolar ADC.

Successive-Approximation Register ADC Design

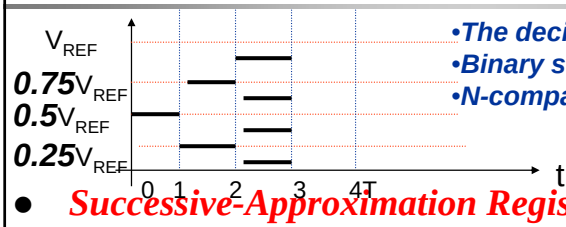
Ron-Yi Liu

- ***First step Approximation Sequence:* Sampling Input, then Digital control circuits assume only MSB=1 to DAC (=0.5V_{REF}). Compare with input again, if X is high then MSB=1 otherwise MSB=0 as *N cycle for N-bit*.**



- ***Then MSB=1 known, then the approximation process continues by once again a guess digital word to DAC.***

Successive-Approximation Register ADC Design

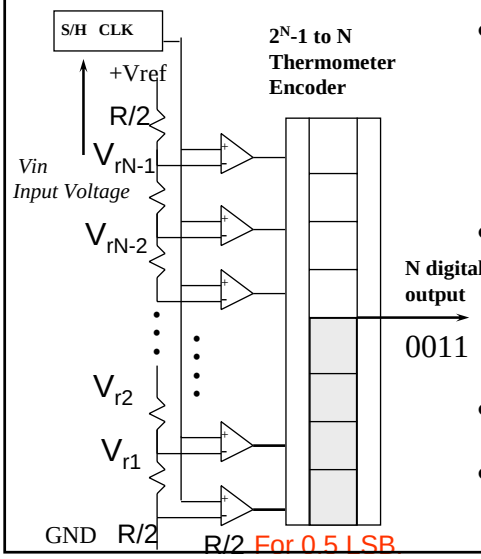


- *The decision sequence.*
- *Binary search for possible subregions.*
- *N-comparisons per conversion.*

- ***Successive-Approximation Register (SAR) ADC :***

  Most popular ADC because it offers high accuracy and moderate conversion speed.
- ***Trial-and-error feedback '"guess" scheme to approximate each analog sample with a digital word as $V_{DAC}= (b_1 V_{FS}/2 + b_2 V_{FS}/4 +\ldots\ )$.***
- ***In each cycle, if the error (between sampling input and DAC output) is positive, the bit is high; otherwise it is returned to zero.***
- ***Compatible to bit-slice operation.***

Flash (Parallel) ADC



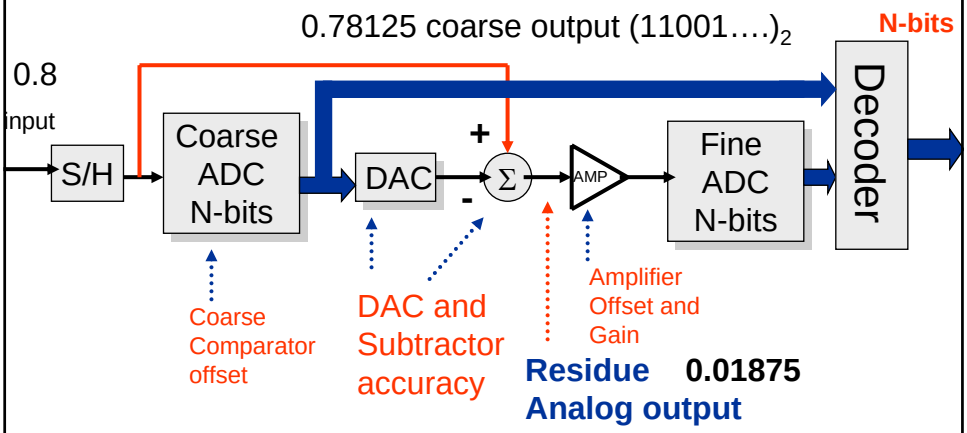
- ***Advantages :***
  - ✓ ***Requires only one comparison cycle per conversion. ⇒ Very High speed converter for video signal processing.***
  - ✓ ***All sub-regions are examined simultaneously.***
- ***Disadvantages :***
  - ✓ **Need 2^N –1 resistors and comparators in parallel⇒ Large area and power.**

    ⇐CMOS inverter for small clocked Comparator.
- ***Maybe One more comparator for detecting the overflow condition.***
- ***Need simple 3-input NAND gates to check more than one bubble error such as 0,0, 1, 0, 1,1, 1, 1,...***

Two-Step (Subranging) ADC Architecture

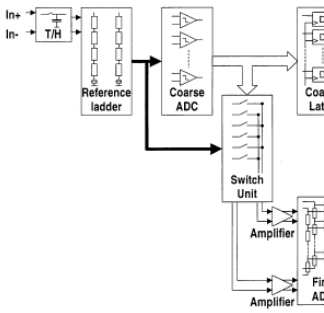
Ron-Yi Liu

- *Quantized Feedford (Subranging) Architectures* :



Subranging ADC Chip and Measurement

Ron-Yi Liu



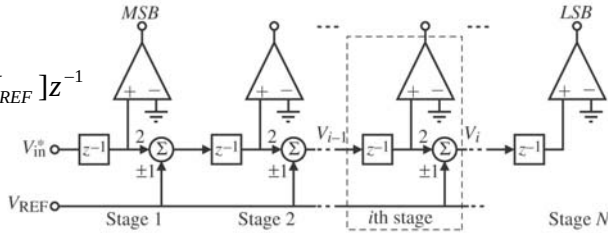
Technology	Single Poly 0.35 μm CMOS
Resolution	10 bits
Supply Voltage	3.3 Volt
Conversion Rate	25 MSample/s
Input Range	1.6 V_{PP} differential
Resolution Bandwidth	12 MHz (25 MS/s)
Effective Number of Bits	9
Signal-to-Noise Ratio	58 dB
Total Harmonic Distortion	-62 dB
Spurious Free Dynamic Range	72 dB
Integral-non-Linearity	0.9 LSB
Differential-non-Linearity	0.7 LSB
Power Dissipation	195 mW
Area	0.66 mm^2

(F_{IN}= 1 MHz, F_S= 25 MS/s)

Pipeline Algorithmic ADC Design

iterative ADC:

$$V_{oi} = [2V_{o.i-1} - b_i V_{REF}]z^{-1}$$



Operation:

•Each stage multiplies its input by 2 and adds or subtracts V_{REF} depending upon the sign of the input **(like iterative ADC)**.

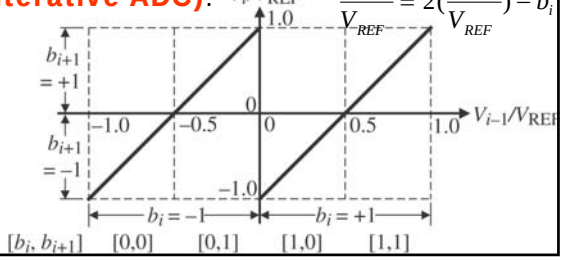
$$\frac{V_{o.i}}{V_{REF}} = 2\left(\frac{V_{o.i-1}}{V_{REF}}\right) - b_i$$

• *i-th* stage :

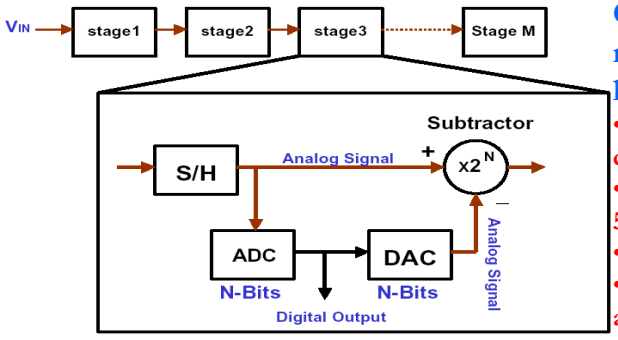
$$V_i = 2V_{i-1} - b_i V_{REF}$$

where b_i is given as

$$b_i = \begin{cases} +1 \text{ if } V_{i-1} > 0 \\ -1 \text{ if } V_{i-1} < 0 \end{cases}$$



Pipeline ADC Architecture



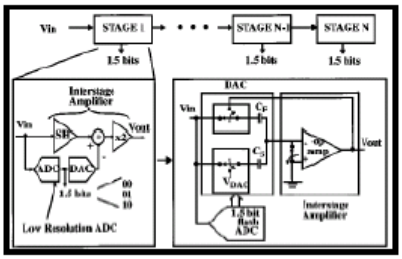
Cascade of low resolution stages for higher conversion speed

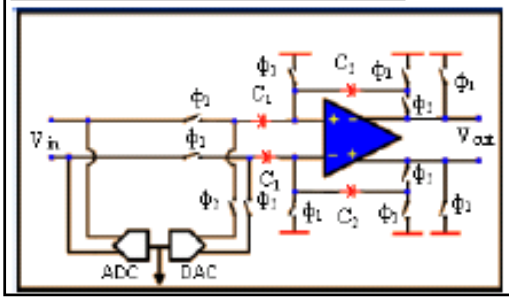
- Stages operate concurrently- trades latency
- Sampling rate : 50 MHz - 200 MHz
- Resolution : 8b - 15b.
- Low power consumption and small chip area.

- **Input accuracy limited by R and C of input switches (first stage).**
- **Conversion speed limited by interstage amplifiers with high gain.**
- **Full performance evaluation affected by high operating frequency.**

1.5 b/stage MDAC (Multiplying DAC)

Ron-Yi Liu





Phase 1:

$$Q = C_1 * V_{in} \qquad (4)$$

Phase 2:

$$Q = (V_{DAC} - V_x)C_1 + (V_x - V_{out})C_2 \qquad (5)$$

Where V_{DAC} is the output of the DAC, A is the op amp gain and V_x is the input voltage of the op amp and thus, $V_x = -\frac{Vout}{A}$.

From (4) and (5),

$$(V_{DAC} - V_x)C_1 + (V_x - V_{out})C_2 = C_1 * V_{in}$$

$$\frac{V_{out}}{V_{in} - V_{DAC}} = \frac{C_1}{\frac{C_1}{A} - \frac{C_2}{A} - C_2}$$

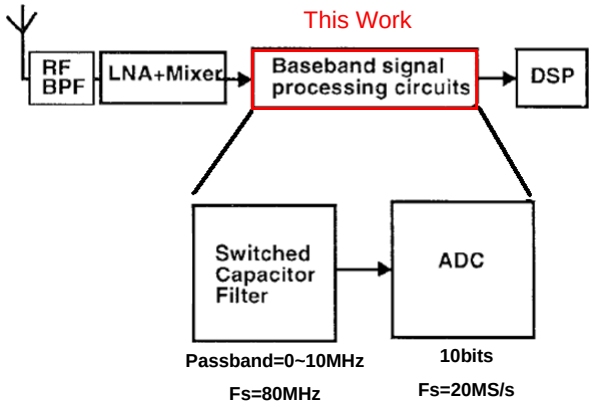
For a large A,

$$\frac{V_{out}}{V_{in} - V_{DAC}} \approx -\frac{C_1}{C_2} \qquad (6)$$

■**Subtraction, S-H and 2x (gain-of-2) Gain circuit.**

Block Diagram of WiMAX Chip Design

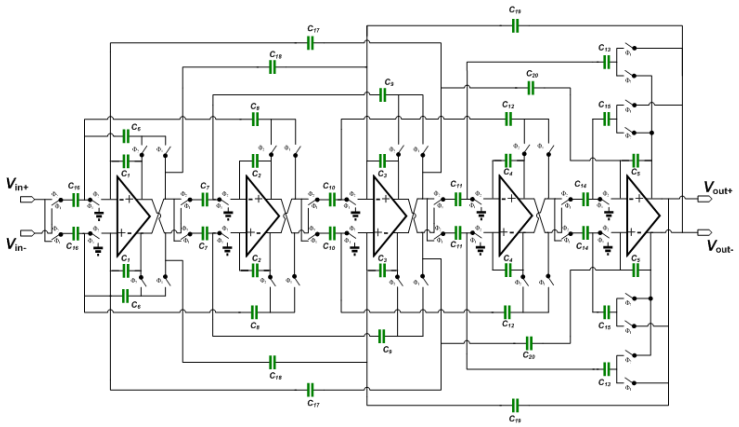
Ron-Yi Liu



No sample-and-Hold circuit.

Switched-Capacitor Filter

Ron-Yi Liu



Capacitor Table

Ron-Yi Liu

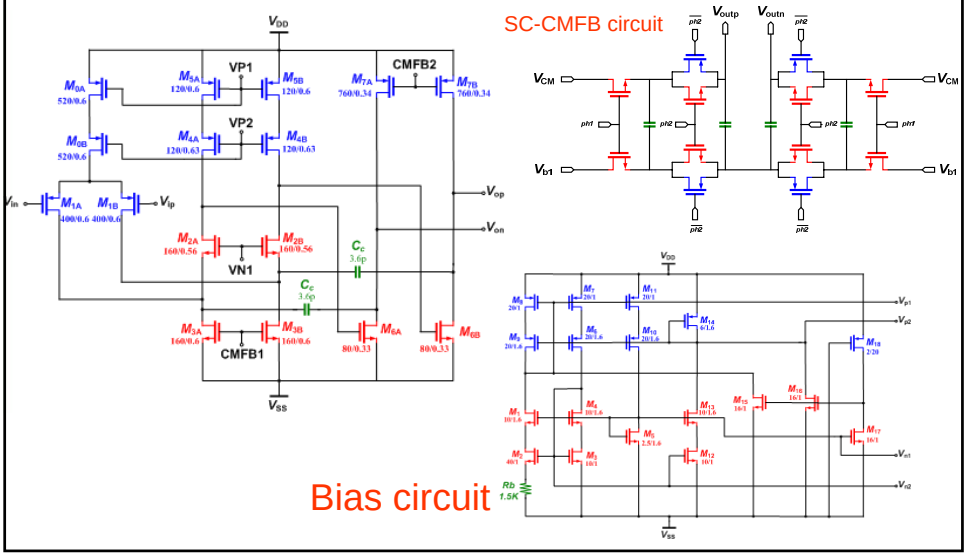
Cap. No.	w/o any scaling	After Dynamic Range Scaling	After Minimum Cap. Scaling	Layout Cap. (unit cap.=0.4pF)
C1	1	0.87	4.57	1.828p
C2	1	1.54	4.18	1.672p
C3	1	0.83	31	12.4p
C4	1	1.01	6.21	2.284p
C5	1	0.47	6.85	2.74p
C6	0.285	0.11	1.22	0.488p
C7	0.382	0.18	1.05	0.42p
C8	0.285	0.195	2.06	0.824p
C9	0.382	0.176	1	0.4p
C10	0.117	0.121	9.4	3.76p
C11	0.299	0.142	1.68	0.672p
C12	0.117	0.08	6.2	2.48p
C13	0.299	0.085	1	0.4p
C14	0.187	0.133	3.775	1.51p
C15	0.187	0.066	1.89	0.756p
C16	0.285	0.126	1.36	0.544p
C17	0.285	0.223	1	0.4p
C18	0.188	0.146	4.9	1.96p
C19	0.067	0.028	1	0.4p
C20	0.106	0.01	1	0.4p

Cap. Spread=

Cmax/Cmin=31

Op Amp Circuit in SCF

Ron-Yi Liu



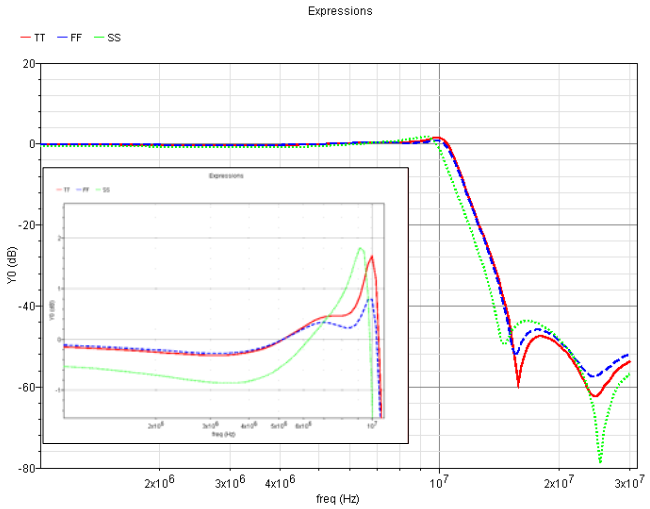
Specification of Op Amp Circuit

Ron-Yi Liu

	SPEC.	Pre-Simulation
Power Supply(Volts)	-0.9~0.9	-0.9
Open Loop Gain(dB)	≧60	90.83
Unity Gain BW(MHz)	≧75	452.5
Phase Margin(°)	≧60	62.77
Output Swing(Volts)	>±1	1.67
VOS(Volts)	Minimum	1.523
ICMR(Volts)	-1~2	0.6179
CMRR(dB)	Maximum	111.8
PSRR(dB)	Maximum	109.8 / 88.92
Rise Time(ns)	<10	3
Fall Time(ns)	<10	0.59
Slew Rate @ Rise(V/us)	≧10	212.43
Slew Rate @ Fall(V/us)	≧10	1085.25
Setting Time @Rise(us)	Minimum	27n
Setting Time @Fall(us)	Minimum	6n
Noise @1KHz (V^2 / Hz)	Minimum	4.28*10-6
Noise @10KHz (V^2 / Hz)	Minimum	2.573*10-7
Noise @100KHz (V^2 / Hz)	Minimum	8.043*10-10
Total Harmonic Distortion(%)	Minimum	4.56
Power Dissipation(mW)	Minimum	5.3

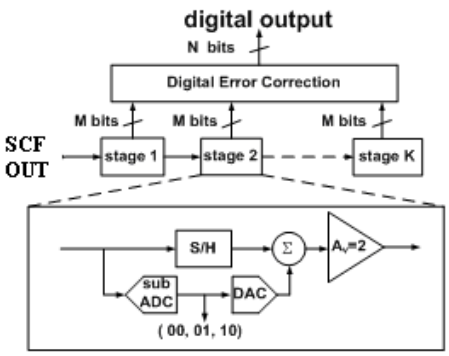
Frequency Response of SCF by SpectreRF (Corner simulation)

Ron-Yi Liu



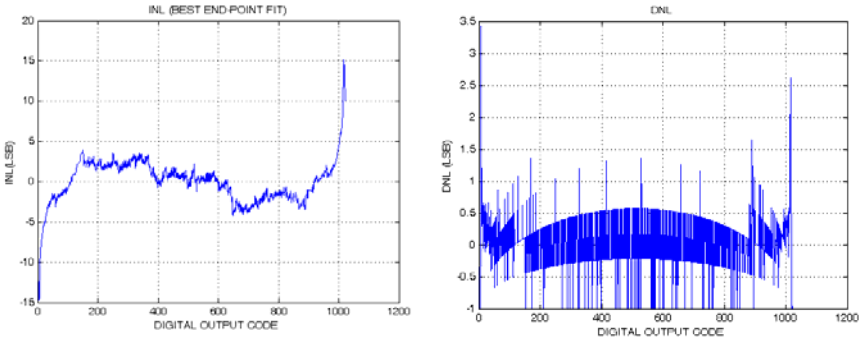
The Structure of Pipelined ADC

Ron-Yi Liu



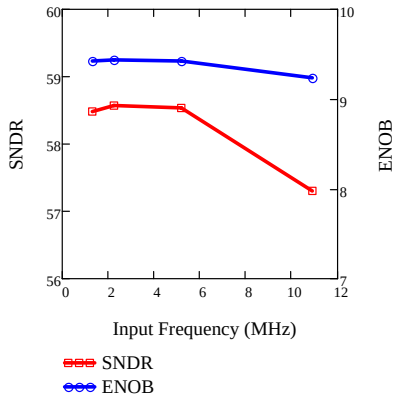
INL & DNL

Ron-Yi Liu



SNDR and ENOB

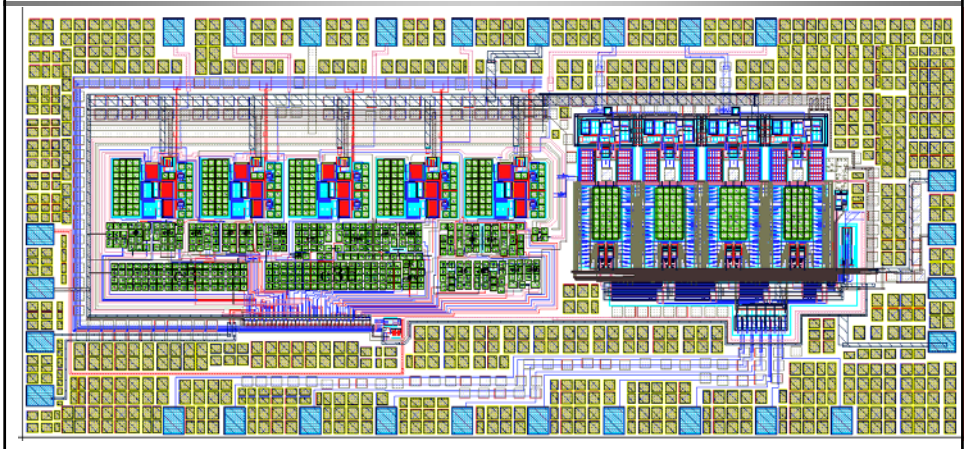
Ron-Yi Liu



Overall Chip Layout

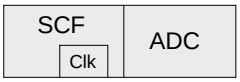
2010/5/3

Ron-Yi Liu



Area: 2730um x 1207um

Floor Plan



Overall Circuit Simulation

Output Code

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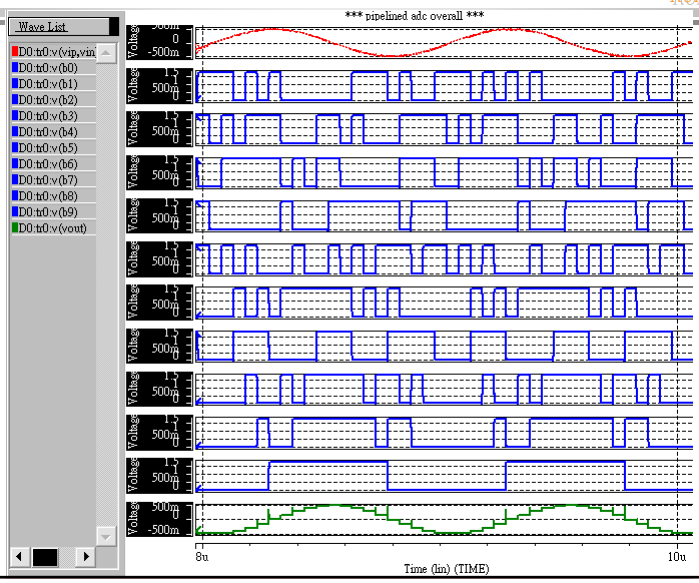
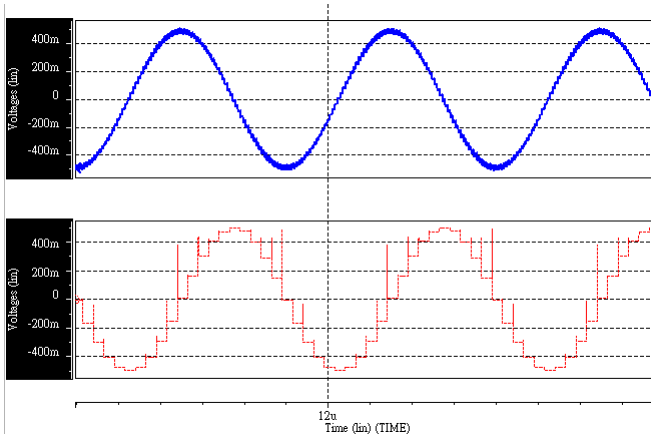


Overall Circuit Simulation

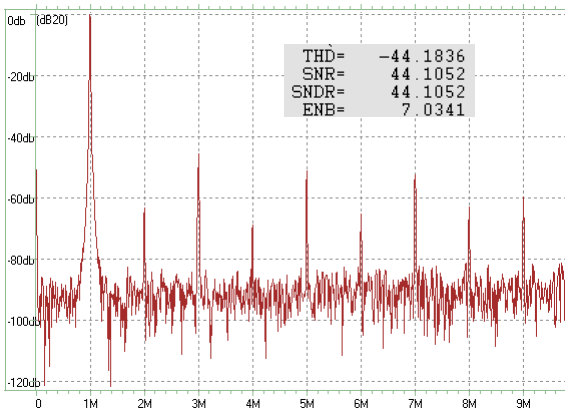
Reconstruction Result (input=1.31MHz)

Ron-Yi Liu



FFT(Fin=1MHz, 2048 points)

Ron-Yi Liu



Thanks for your attention !